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[AFRICON, 1999 IEEE](#)
Volume 1, 28 Sept.-1 Oct. 1999 Page(s):501 - 506 vol.1
Digital Object Identifier 10.1109/AFRCON.1999.820933
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VCO. X. s(t). e(t). v(t). Figure 3.1: Simple illustrative **PLL** model. = $-\cos(\omega \dots$ phase detector (PD) with a **frequency difference detector** (FDD). ...

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A **PLL** with a **digital loop** filter is explored. The main advantage of the DPLL is that it avoids ... phase error by a high frequency clock, such as the **VCO**. ...

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the high-speed BBPLLs implemented up to now use **analog loop** filters, we extend the concept and ... **analog LC VCO**. The frequency resolution of the DCO goes ...

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a **digital loop** filter coupled to the phase-frequency detector including a ... The **VCO** 130 is an analog device. Consequently, the **PLL** 110 can achieve a high ...

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analog loop, acting as in a conventional **PLL**, locks to the. input phase difference. ...

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Listing 6 shows the model of the **digital loop** filter,. 1. 1. UP. DN. T2D. Fref. Fref. PFDout.

DFF. DFF. Figure 4. The digital phase and **frequency detector** ...

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This analog phase-locked loop comprises a phase/frequency detector (PFD), ... the **analog loop** filter can be replaced by any desired type of a **digital loop** ...

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Prior art designs which implement an **analog loop** filter use at least one discrete ... The **PLL** uses a voltage controlled oscillator (**VCO**) in which the output ...

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VCO as integrator makes every **PLL** at least Type 1 ... The combination of a tri-state phase-
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...chips including all building blocks of a **PLL**-based synthesizer except for the voltage...One of the main problems of the integer-N **PLL** based synthesizer when used in a multichannel...Kostamovaara J (1998) A Bipolar Semicustom **PLL** Based Synthesizer for GSM and DCS Systems...
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Oct 1998
...error detector of some sort, which for the **PLL** is a PD, modeled in Figure 3.1 as a multiplier, 2) a loop filter, and 3) a **VCO**. Note that for an AFC loop the error term...THE PHASE-LOCKED LOOP 13 Loop Filter **VCO** X s(t) e(t) v(t) Figure 3.1: Simple illustrative **PLL** model = - cos(ct +) · sin(ct...design progresses. 3.2 Linearized Analog **PLL** Model Assuming that after some convergence...phase domain model of Figure 3.2 where the **VCO** is modeled as a perfect integrator with...
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☐ 6. Direct digital frequency synthesis enabling spur elimination

Sander, Wendell / Sander, Brian, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jul 2000


...voltage-controlled oscillator (**VCO**). Finally, an output of the **VCO** is input to the...As compared to a **PLL** using a conventional phase/**frequency detector** (PFD), the **PLL**...a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage...controlled oscillator (**VCO**). In FIG. 3, the...

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☐ 7. DIRECT DIGITAL FREQUENCY SYNTHESIS ENABLING SPUR ELIMINATION

SANDER, Brian / SANDER, Wendell, EUROPEAN PATENT, Jun 2002


...a conventional **PLL** structure including a phase/**frequency detector** (PFD), an **analog loop** filter and a voltage...controlled oscillator (**VCO**). In Figure 3...controlled oscillator (**VCO**). Finally, an output of the **VCO** is input to the...As compared to a **PLL** using a conventional phase/**frequency detector** (PFD), the **PLL**...

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☐ 8. Phase locked loop using digital loop filter and digitally controlled oscillator

May, Michael R. / Cave, Michael D., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Mar 1998

...Phase-Locked Loops (**PLL**) are one type of oscillator...and memory devices. **PLL**'s synchronize output...controlled oscillator (**VCO**) synchronizing clock...block diagram of a **digital loop** filter illustrated...provides as input to the **digital loop** filter 12. The RANDOM...A Type IV phase and **frequency detector** 21 connects to a D...

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☐ 9. Modulation and frequency synthesis for wireless digital radio

Bax, Walter T., Jan 2000

...120 4.2.3 Phase-**Frequency Detector**...4.37 Phase-**frequency detector** with asynchronous reset 130...132 4.10 Differential phase-**frequency detector** transfer function...

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☐ 10. Timing control for PRML class IV sampling data detection channel


Johnson, Kenneth E. / Abbott, William L. / Nguyen, Hung C., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Nov 1993

...controlled oscillator (**VCO**). Logic gating at...transition edges. The **PLL** operating frequency...PR4,ML system, a **PLL** has been needed...Separate phase/**frequency detector** circuits must be...selected to control the **PLL** oscillator frequency...approach, a common **analog loop** compensation filter...facilitate the use of a **digital loop** filter during READ...


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- ☐ **12. [Zero phase start optimization using mean squared error in a PRML recording channel](#)**
Ziperovich, Pablo A. / Chiao, James, EUROPEAN PATENT APPLICATION, Mar 1996
...a phase locked loop ("**PLL**") to generate a coherent...mode is entered, the **PLL**, typically acquires the...controlled oscillator ("**VCO**") has had an ENABLE input...output by the timing loop **VCO** coincided at the input to the phase-**frequency detector** simultaneously, or nearly...error was near zero, and **PLL** acquisition time was...
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- ☐ **14. [Zero phase start optimization using mean squared error in a PRML recording channel](#)**
Ziperovich, Pablo A. / Chiao, James, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Sep 1996
...charge pump 270 passes into an **analog loop** low pass filter 274. The loop...analog charge pump 270 and the **analog loop** filter 274. Thus, during non-read...detector 268, charge pump 270, **analog loop** filter 274 and buffer 260...the frequency synthesizer **PLL** 262. Ordinarily, the timing...
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- ☐ **15. [Digital filtering, data rate conversion and modem design](#)**
Terrell, Peter M., **UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT**, Mar 1996
A digital filter 23 receives a control signal which specifies what filter coefficient values should be used. The control signal can be changed repeatedly so as to dynamically select the coefficients in response to the value of a control parameter. The ...
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- 17. [AN INVESTIGATION OF CARRIER RECOVERY](#) [PDF-316K]**



Jun 1997

...submit. v 3.6 The Notion of Optimality for a **PLL**...Example of a feedback control system: A simple **PLL** model 6 1.3 Example open-loop...7 3.1 Simple illustrative **PLL** model...

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Meltzer, D.; Mandel, L.;
[Quantum Electronics, IEEE Journal of](#)
Volume 6, Issue 11, Nov 1970 Page(s):661 - 668
[Abstract](#) | Full Text: [PDF\(872 KB\)](#) IEEE JNL
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- ☐ 2. **Authors' Reply²**
Lackey, R.B.; Meltzer, D.;
[Computers, IEEE Transactions on](#)
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- ☐ 3. **A Simplified Definition of Walsh Functions**
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[Computers, IEEE Transactions on](#)
Volume C-20, Issue 2, Feb. 1971 Page(s):211 - 213
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- ☐ 4. **A 1.0-GHz single-issue 64-bit powerPC integer processor**
Silberman, J.; Aoki, N.; Boerstler, D.; Burns, J.L.; Sang Dhong; Essbaum, A.; C
Heidel, D.; Hofstee, P.; Kyung Tek Lee; Meltzer, D.; Hung Ngo; Nowka, K.; Po
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[Solid-State Circuits, IEEE Journal of](#)
Volume 33, Issue 11, Nov. 1998 Page(s):1600 - 1608
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S.D.; Takahashi, O.;
[Micro, IEEE](#)
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Posluszny, S.; Aoki, N.; Boerstler, D.; Coulman, P.; Dhong, S.; Flachs, B.; Hofst
N.; Kwon, O.; Lee, K.; Meltzer, D.; Nowka, K.; Park, J.; Peter, J.; Silberman, J.;
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Zyuban, V.; Meltzer, D.;
[Low Power Electronics and Design, International Symposium on, 2001.](#)
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Hofstee, P.; Aoki, N.; Boerstler, D.; Coulman, P.; Dhong, S.; Flachs, B.; Kojima
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[Abstract](#) | [Full Text: PDF\(250 KB\)](#) IEEE CNF
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9. **Trends in compilable DSP architecture**
Glossner, J.; Moreno, J.; Moudgill, M.; Derby, J.; Hokenek, E.; Meltzer, D.; Shv
M.;
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11-13 Oct. 2000 Page(s):181 - 199
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Posluszny, S.; Aoki, N.; Boerstler, D.; Burns, J.; Dhong, S.; Ghoshal, U.; Hofst
D.; Lee, K.; Meltzer, D.; Ngo, H.; Nowka, K.; Silberman, J.; Takahashi, O.; Vo,
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11. **A 1.0 GHz single-issue 64 b powerPC integer processor**
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D.; Hofstee, P.; Lee, K.; Meltzer, D.; Ngo, H.; Nowka, K.; Posluszny, S.; Takah
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Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on Circuits and Systems I: Regular Papers, IEEE Transactions on
 Volume 49, Issue 9, Sep 2002 Page(s):1309 - 1316
 Digital Object Identifier 10.1109/TCSI.2002.802347
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 De Muer, B.; Steyaert, M.S.J.;
Solid-State Circuits, IEEE Journal of
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- ☐ 3. **Design and implementation of a low-phase-noise integrated CMOS Frequency Synthesizer for high-sensitivity narrow-band FM transceivers**
 Kamal, M.M.; El-Shewekh, E.W.; El-Saba, M.H.;
Microelectronics, 2003. ICM 2003. Proceedings of the 15th International Conference 9-11 Dec. 2003
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 Kuo-Hsing Chen; Huan-Sen Liao; Lin-Jiunn Tzou;
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